REMARKS

Applicant provides the present *Amendment* in response to the Office Action of September 5, 2005. As an initial matter, Applicant wishes to acknowledge the thorough search of the prior art evidenced by the search history report included with the September 8, 2005 Office Action. Applicant also wishes to thank the Examiner for the withdrawal of the previously issued (see the Office Action dated January 25, 2005) rejections of Claims 1, 3-9 and 11-13 based on U.S. Patent No. 5,636,173 to Schaefer. The September 8, 2005 Office Action, however, includes new rejections of each of the pending claims based on U.S. Patent No. 6,571,325 to Satagopan et al. ("Satagopan"). As discussed below, a careful review of Satagopan reveals that it does not disclose or suggest the inventions of Claims 1-12 or 16-24. Accordingly, for at least the reasons discussed below, Applicant respectfully submits that all of the pending claims are in condition for allowance.

II. The Claim Amendments

Independent Claim 1 has been amended to make clear that the auto-precharge function that is included in the command recited in the first clause of the body of Claim 1 is a command for auto-precharging the bank of memory cells that is referred to in the last clause of Claim 1. Dependent Claims 2-4 have been amended to conform with the language of Claim 1. Independent Claim 21 has been amended to correct a typographical error. Independent Claims 7, 12 and 16 remain in their original state as filed.

III. The Rejection of Independent Claim 1

Claims 1-12 and 16-24 stand rejected under 35 U.S.C. § 102(b) as anticipated by Satagopan. Claim 1 recites:

> 1. A method of precharging a semiconductor memory device, the method comprising:
>
> receiving a command that includes an auto-precharge function for a bank of memory cells in the semiconductor memory device;

performing the command except for the auto-precharge function;

initiating a timer in response to the received command; and

performing the auto-precharge function for automatically precharging the bank of memory cells responsive to the timer reaching a predetermined value.

The Office Action states that Table 1 and Col. 12, lines 47-64 of Satagopan discloses the method of Claim 1. Applicant respectfully traverses this rejection.

Satagopan describes a memory controller 500 that may be used to control a memory system 200. As explained with respect to Table 1 of Satagopan, the memory system 200 may have known timing constraints. These constraints are defined in terms of the delay required after issuance of a first command (e.g., an Activate, Read/Write or Precharge command) before a second command may be acted upon. As Table 1 of Satagopan makes clear, the memory controller 500 of Satagopan ensures that specified minimum delay times are provided **between issuance of the first command and the subsequent second command**. Thus, for example, constraint T_{red} of Table 1 of Satagopan specifies that after an Activate command is issued, a delay of at least 20 ns is required before a Read/Write command may be issued to the same page within the memory device. (Satagopan at Col. 11, lines 51-54). Every other delay specified in Table 1 of Satagopan likewise specifies a delay required between issuance of a first command and a second, different command.

In contrast, the method of Claim 1 recites that a timer is initiated "in response to the received command." The "received command" of Claim 1 is the "command that includes an auto-precharge function for a bank of memory cells" that is referenced in the first clause of the body of Claim 1. Claim 1 recites that this received command is performed "except [for] the auto-precharge function." Claim 1 further recites "performing the auto-precharge function for automatically precharging the bank of memory cells responsive to the timer reaching a predetermined value." Thus, according to the method of Claim 1, after the command is received, the command is performed, except for the auto-precharge function, and a timer is initiated. The bank of memory cells associated with the auto-precharge function is thereafter automatically precharged in response to the timer reaching a predetermined value.

As should be clear from the above discussion, in **the methods of Claim 1, the time period between initiation of the timer and the timer reaching the predetermined value determines when the auto-precharge portion of the received command may be carried out, whereas in the system of Satagopan, the delay specifies the time required after issuance of a first command before a second, different command may be issued. Satogopan likewise does not disclose or suggest performing the command except for the auto-precharge function and thereafter performing the auto-precharge function responsive to a timer reaching a predetermined value.** As such, Satagopan simply has no relevance to the methods of Claim 1, and the rejection of Claim 1 as anticipated by Satagopan should be withdrawn for at least these reasons.

IV. The Rejections of Independent Claims 7, 12, 16 and 21

Claim 7 is directed to a semiconductor memory device that includes a precharge control unit that is "configured to issue a precharge control signal to the memory cell array responsive to receipt of a command that includes an auto-precharge function a predetermined time after the command is received." As should be clear from the discussion in the preceding section, Satagopan does not disclose or suggest waiting for a predetermined period of time before issuing a precharge control signal to a bank of the memory device in response to receipt of a command that includes an auto-precharge function for the bank at issue. Instead, the cited portion of Satagopan discloses setting a timer after issuing a **first** command and then not implementing a **second** command until after the timer has cleared. Accordingly, the rejection of Claim 7 should be withdrawn for at least this reason.

Claim 12 is directed to methods of precharging a bank of memory cells in which a timer is initiated in response to receipt of a "read command that includes an auto-precharge function." The read operation is performed, but initiation of the auto-precharge function is delayed until the timer reaches a predetermined time. Applicant respectfully submits that Satgopan does not disclose receiving a read command that includes an auto-precharge function. In fact, Table 1 of Satagopan clearly shows that the read commands and precharge commands used in the system of Satagopan are separate and distinct commands. Moreover,

the cited partions of Satagopan clearly do not disclose or suggest receiving an auto-precharge command but then delaying initiation of the auto-precharge operation until a timer reaches a predetermined time. While a timer is set in response to receipt of a first command, that timer is only used to determine when the system can process subsequent commands – the timer is not used to delay initiation of an operation called for by the first command. Accordingly, the rejection of independent Claim 12 should be withdrawn for at least these reasons.

Claim 16 is directed to a semiconductor memory device that includes "a precharge control circuit that includes at least one timer that is reset in response to the auto-precharge control signal and that initiates precharging of at least a part of the memory cell array when the at least one timer reaches a predetermined value." In the device of Claim 16, the precharge control signal is activated "when a decoded command includes an auto-precharge function." Claim 21 similarly is directed to a semiconductor memory device in which a timer is reset in response to an auto-precharge control signal, and the selected memory banks are precharged when the timer reaches a predetermined value. While the system of Satagopan may reset a timer when a first received command is a precharge command, the system starts to **immediately precharge** the memory cells and the timer is only used to determine when a subsequent command (e.g., a read command) may be processed. Accordingly, Satagopan likewise fails to disclose or suggest the systems of either Claims 16 or 21 and, as such, the rejections of Claims 16 and 21 should also be withdrawn for at least this reason.

V. The Dependent Claims are Patentable Over Satagopan

As shown above, each of the pending independent claims are patentably distinct over Satagopan. Accordingly, dependent Claims 2-6, 8-11, 17-20 and 21-24 are patentable at least as depending from a patentable base claim. Applicants, however, also respectfully submit that the dependent claims are also patentable in their own right over Satagopan.

For example, dependent Claim 2 recites, among other things, "resetting the timer when prior to the timer reaching the predetermined value a second command is received by the semiconductor memory device that is associated with additional data stored in the specific row of the bank." The Office Action cites to Col. 11, line 34 through Col. 12, line 22 of

Satagopan as disclosing this recitation of Claim 2. Applicant, however, has carefully reviewed the cited portion of Satagopan and respectfully submits that it does not disclose the recitations of Claim 2. In fact, there does not appear to be any discussion in the cited passage of resetting a timer prior to the timer expiring for any reason. Thus, Claim 2 is independently patentable over Satagopan for at least this reason.

Similarly, dependent Claim 3 recites that the bank is precharged **prior to the timer reaching the predetermined value**. While the Office Action cites to Col. 12, lines 51-65 of Satagopan as disclosing this recitation of Claim 3, in fact what the cited portion of Satagopan states is that the command is **not** "sequenced" (i.e., carried out) until **after the timer times out**. Accordingly, it is equally clear that Claim 3 is independently patentable over the cited art for at least this additional reason.

In light of the clear distinctions between the pending independent claims and Satagopan, Applicant will not address here how the remaining dependent claims are independently patentable over Satagopan, but instead merely provides such a showing with respect to Claims 2 and 3 as examples.

VI. Conclusion

Applicant again wishes to thank the Examiner for the thorough examination of the application. Applicant believes that, for the reasons discussed above, the claims are all in condition for allowance, which is respectfully requested. Should the Examiner have any questions, please feel free to call Applicants representative at (919) 854-1422.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 28, 2005.

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